WHAT IS CLAIMED IS:

1. A slicing circuit comprising:

a control recording unit which exchanges data with a data bus;

a memory which temporarily stores character broadcasting data extracted from the data bus;

an A/D converter which receives a composite video signal, and converts the composite signal into digital values;

a digital arithmetic and logic unit which receives the digital values converted by the A/D converter, calculates character broadcasting data, and outputs the character broadcasting data to the memory;

a SYNC separator which receives the composite video signal, and extracts a vertical or horizontal synchronizing signal;

a clock generating unit; and

a timing control circuit which receives the output of the SYNC separator, clock generating unit and control recording unit, output to the memory and digital arithmetic and logic unit, and controls a timing.

2. The slicing circuit according to claim 1, wherein the digital arithmetic and logic unit includes,

a plurality of latch circuits;

an arithmetic processing control circuit which receives a sampling clock and a slicing clock, and outputs a first through fourth control signals that show a timing in a one-bit data width;

a first integrator connected to one of the plurality of latch circuits, which first integrator receives the second control signal;

a second integrator connected to a latch circuit, to which the first integrator is not connected, out of the plurality of latch circuits, which second integrator receives the third control signal;

a first adder which receives the output of the first and second integrators;

a third integrator connected to a latch circuit, to which the first and second integrators are not connected, out of the plurality of latch circuits, which third integrator receives the first control signal;

a second adder which receives the output of the third and first adders; and

a correcting circuit which receives the output of the second adder and the fourth control signal.

3. The slicing circuit according to claim 1, wherein the digital arithmetic and logic unit includes,

a plurality of latch circuits;

an arithmetic processing control circuit which receives a sampling clock and a slicing clock, and outputs a first through fourth control signals that show a timing in a one-bit data width;

a first selector connected to at least two latch circuits out of the plurality of latch circuits, which first selector receives the first control signal;

a second selector connected to at least two latch circuits, to which the first selector is not connected, out of the plurality of latch circuits, which second selector receives the second control signal;

a first adder which receives the output of the first and second selectors;

an integrator connected to at least two latch circuits, to which the first and second selectors are not connected, out of the plurality of latch circuits;

a second adder which receives the output of the integrator and first adder; and

a correcting circuit which receives the output of the second adder.

4. A slicing circuit for arithmetically correcting character broadcasting data extracted from a composite video signal, the slicing circuit comprising:

an arithmetic processing unit which changes over an

arithmetic processing at a sampling timing of the composite video signal.